RALPH
MCELROY TRANSLATION
COMPANY

March 8, 2004

Re: 844-97248

To Whom It May Concern:

This is to certify that a professional translator on our staff who is skilled in the Japanese language translated the enclosed Kokai Patent Application No. Sho 62[1987]-30323 from Japanese into English.

We certify that the attached English translation conforms essentially to the original Japanese language.

Kim Vitray
Operations Manager

Subscribed and sworn to before me this 8th day of March, 2004

TINA WUELFING
Notary Public
State of Texas
My Commission Expires
December 8, 2007

Tina Wuelfing
Notary Public

910 WEST AVE.
AUSTIN, TEXAS 78701
www.mcelroytranslation.com

(512) 472-6753
1-800-531-9977
FAX (512) 472-4591

Japanese Kokai Patent Application No. Sho 62[1987]-30323

Job No.: 844-97248 Ref.: TIJ-24816 US
Translated from Japanese by the Ralph McElroy Translation Company
910 West Avenue, Austin, Texas 78701 USA

JAPANESE PATENT OFFICE
PATENT JOURNAL (A)
KOKAI PATENT APPLICATION NO. SHO 62[1987]-30323

Int. Cl.[4]:	H 01 L 21/302 21/306
Sequence Nos. for Office Use:	A-8223-5F Z-8223-5F J-8223-5F B-8223-5F
Filing No.:	Sho 60[1985]-168902
Filing Date:	July 31, 1985
Publication Date:	February 9, 1987
No. of Inventions:	1 (Total of 5 pages)
Examination Request:	Not filed

FINE PROCESSING METHOD

Inventors:	Keiji Horioka Toshiba Corp. General Research Lab. 1 Toshiba-cho, Komukai, Saiwai-ku Kawasaki-shi Haruo Okano Toshiba Corp. General Research Lab. 1 Toshiba-cho, Komukai, Saiwai-ku Kawasaki-shi
Applicant:	Toshiba Corp. 72 Horikawa-cho, Saiwai-ku Kawasaki-shi, Kanagawa-ken
Agents:	Takehiko Suzue, patent attorney, and 2 others

[There are no amendments to this patent.]

Claims

1. A fine processing method characterized in that it includes a step in which an etching mask is formed on a workpiece, a step in which a thin film is formed over the entire surface of the aforementioned workpiece and the etching mask, a step in which full-surface etching is applied to the aforementioned thin film in such a way that said thin film remains only on the side walls of the aforementioned etching mask, and a step in which the aforementioned thin film and the workpiece are selectively etched using an etching containing no charged particles with the aforementioned etching mask as a mask.

2. The fine processing method of Claim 1, characterized in that electrically neutral halogen radicals generated by means of optical pumping or electric discharge pumping are used in the step in which the aforementioned thin film and the workpiece are etched.

3. The fine processing method of Claim 1, characterized in that an acid or alkali solution is used in the step in which the aforementioned thin film and the workpiece are etched.

4. The fine processing method of Claim 1, characterized in that the etching is carried out under etching conditions whereby the aforementioned thin film and the workpiece are etched at approximately the same rate.

5. The fine processing method of Claim 1, characterized in that a monocrystalline silicon substrate is used as the aforementioned workpiece, a silicon oxide film or a silicon nitride film is used as the aforementioned etching mask, and a polycrystalline silicon film is used as the aforementioned thin film.

Detailed explanation of the invention

Industrial application field

The present invention pertains to a fine processing method used for manufacturing semiconductor integrated circuits. In particular, it pertains to a fine processing method for realizing etching without damage or undercutting.

Technical background and its problems

As semiconductor integrated circuits became more highly integrated, etching methods underwent a transition from wet etching utilizing alkali solutions to plasma etching utilizing reactions with active species in a plasma, so that recently reactive ion etching and reactive ion beam etching have become the predominant etching methods. Reactive ion etching and reactive ion beam etching are referred to as anisotropic etching, which is characteristic in that orthogonal etching along the mask is realized utilizing the reaction promoting effect of the ions incident perpendicular to the substrate surface. In other words, as shown in Figure 4 (a), when a sample is used in which etching mask 42 made of a silicon oxide is formed on silicon substrate 41, silicon

substrate 41 can be etched orthogonally along mask 42 as shown in (b) of said figure, so that groove 43 with vertical side walls can be formed. As a result, the problem of dimensional conversion errors due to undercutting can be eliminated, thereby making a significant contribution to the achievement of a higher level of integration.

On the other hand, with said methods, because the workpiece is directly exposed directly to charged particles, such as ions and electrons, there is the problem that dielectric breakdown of the insulating film and/or crystal defects in the substrate semiconductor may be induced. In order to solve this problem, a down-flow type etching device in which the plasma discharge part is separated from the etching chamber, and electrically neutral halogen radicals are used for etching has been developed. However, with this method, as shown in Figure 4 (c), undercutting cannot be eliminated. While in the meantime, an attempt has been made to carry out damage-free anisotropic etching utilizing optical excitation reaction, it has not yet reached a practical level.

On the other hand, when etching monocrystalline silicon with <100> surface using an alkali solution, the etching rate is dependent on the orientation of the crystal surface, and <100> surface is hardly etched. Thus, the tapered etched shape with no undercut shown in Figure 4 (d) results. However, because surface (110) is etched at a fixed rate in the 45° direction relative to it, an undercut is unavoidable as shown in Figure 4 (e).

In addition, there are cases in which a tapered etched shape is preferred over a vertical shape depending on the step. For example, first polysilicon during a 2-layer polysilicon process and etching of monocrystalline silicon during the formation of an embedded element separation area may be mentioned. In particular, in the case of the monocrystalline silicon etching process, dimensional conversion errors with respect to the bottom part caused by the etching do not create any problems. Rather, there are demands for the development of an etching method free of undercutting and damage.

Objective of the invention

The present invention was conceived in light of the aforementioned situation, and its objective is to present a fine processing method suitable for manufacturing a semiconductor integrated circuit with which etching can take place with no undercutting or damage due to charged particles.

Outline of the invention

The main point of the present invention is that a thin film of prescribed thickness is formed on the side walls of the etching mask in advance in order to improve etching results when wet etching or neutral radicals are used.

That is, the present invention is a fine processing method for forming a groove by etching the workpiece, wherein, after an etching mask is formed on a workpiece, a thin film is formed over the entire surface of the aforementioned workpiece and the etching mask, full-surface etching is then applied to the aforementioned thin film in such a way that said thin film remains only on the side parts of the aforementioned etching mask, and selective etching is then applied to the aforementioned thin film and the workpiece using an etchant containing no charged particles while using the aforementioned etching mask as a mask.

Effect of the invention

In the present invention, an etched shape along the mask can be attained without dimensional conversion errors using an etching means which does not involve emission of charged particles. Thus, the problems of inducing dielectric breakdown of the insulating film and crystal defects associated with conventional reactive ion etching can be eliminated. As a result, when the present invention is applied to the manufacture of semiconductor integrated circuits, the yield and reliability of said semiconductor integrated circuits can be improved.

Application examples of the invention

Details of the present invention will be explained below using application examples illustrated by the attached figures.

Figures 1 (a) through (d) are cross-sectional views of groove formation steps pertaining to the method of an application example of the present invention. First, as shown in Figure 1 (a), an 8000-Å-thick silicon oxide film pattern was formed as etching mask 12 on the <100> surface of monocrystalline silicon substrate (workpiece) 11. Then, an 8000-Å-thick polycrystalline silicon film (thin film) 13 was deposited over the entire surface using CVD as shown in Figure 1 (b). In this case, polycrystalline silicon film 13 is deposited in the direction approximately perpendicular to the substrate surface, and the film becomes thicker near the mask.

Then, as shown in Figure 1 (c), full-surface etching was applied to polycrystalline silicon film 13 using reactive ion etching until silicon oxide film 12 was exposed. At this time, polycrystalline silicon film 13 is left only on the side walls of mask 12.

Then, as shown in Figure 1 (d), selective etching was applied to polycrystalline silicon film 13 and silicon substrate 11 by means of chemical dry etching (CDE), a down-flow type of plasma etching, while using silicon oxide film 12 as the mask. Groove 14 formed on substrate 11 as a result of said etching assumed an arc-like etched form passing through the mask edge, and no dimensional conversion errors occurred. Also, a fluorine gas was used as an etchant during the aforementioned etching.

Here, the reason that the aforementioned etched form can be realized will be explained with reference to Figure 2. The etching of silicon using fluorine radicals is not very dependent on direction or orientation with respect to the surface, and the polycrystalline silicon and the monocrystalline silicon are both etched at the same rate. Thus, the etched form can be represented using a set of envelopes of circles 20, and it is dependent on the width of the polycrystalline silicon remaining on the side walls. For example, Figure 2 (a) will result when said width is equal to the height of the mask, and (b) of said figure will result when the width is greater than the height. Because the width of the film remaining on the side walls can be controlled on the basis of the deposition conditions of the film on the polycrystalline silicon or during the removal of the film, the etched form can be controlled in this way.

Thus, with the method of the present application example, etching along mask 12 can be realized due to electrically neutral fluorine radicals. Thus, an etched form containing no undercutting can be realized without any damage and/or crystal defects due to the emission of charged particles. Therefore, it demonstrates an extraordinary effect when applied to the manufacture of semiconductor integrated circuits.

Next, another application example of the present invention will be explained. In this application example, wet etching is used in place of the aforementioned etching using fluorine radicals.

That is, while it is identical to the aforementioned application example up to the step shown in Figure 1 (c), wet etching equivalent to 8000 Å was applied using an aqueous (isopropylene alcohol) mixture with 40% potassium hydroxide during the steps for etching polycrystalline silicon film 13 and silicon substrate 11. When the etched form was observed, it was found that upper parts of the side walls were tapered, and the bottom part had the form of an arc as shown in Figure 3 in the case of the orientation of the crystal in which the <111> surface appears on the side walls. In addition, it matched the shape shown in Figure 1 (d) as far as the orientation of the <100> surface was concerned. This was due to the fact that the etching rates of the monocrystalline silicon <100> and <110> surfaces and the polycrystalline silicon were almost the same. Thus, no dimensional conversion errors occurred at any orientation.

Thus, with the method of the present invention, an etched shape containing no undercutting can be attained along the mask by means of wet etching. Thus, the same effect as that of the aforementioned application example can be obtained.

Furthermore, the present invention is not restricted to the methods of the aforementioned respective application examples. For example, the aforementioned workpiece is not restricted to monocrystalline silicon but can be applied to polycrystalline silicon, silicon oxide, or aluminum film as well. Furthermore, the etching mask is not restricted to silicon oxide film, but silicon nitride film or any other type of film may be used as long as the etching selectivity with respect

to the workpiece can be assured. In addition, other than polycrystalline silicon, a metal such as aluminum, various types of organic resists, or various types of glass can also be used as the thin film that is to remain on the side walls. Furthermore, the means for the full-surface etching of the thin film is not restricted to reactive ion etching, but reactive ion beam etching, dry etching that uses halogen radicals generated by light or electrical discharge, or wet etching that uses an acid or alkali solution can be used also.

In addition, not only reactive ion etching but reactive ion beam etching, dry etching utilizing halogen radicals generated by light or electric discharge, or wet etching utilizing an alkali solution may also be used for <110>.

As a means of etching the workpiece, other than chemical dry etching, that is, dry etching utilizing halogen radicals excited by means of an electric discharge, a method which utilizes halogen radicals generated by means of optical excitation, may also be used. Furthermore, wet etching utilizing an alkali other than potassium hydroxide or an acidic solution may also be used. In addition, although the case in which the object to be etched and the thin film remaining on the side walls were etched at the same rate was explained in the application examples, the present invention can also be applied to cases in which they are different. Moreover, the present invention can be modified and implemented variously without exceeding the scope thereof.

Brief description of the figures

Figures 1 (a) through (d) are cross-sectional views of groove formation steps pertaining to the method of an application example of the present invention. Figures 2 (a) and (b) are schematic diagrams for illustrating the function of the aforementioned application example. Figure 3 is a cross-sectional view showing the etched shape formed by the method of the present invention in another application example. Figures 4 (a) through (e) are cross-sectional views for explaining the problem of the conventional method.

11 ... monocrystalline silicon substrate (workpiece); 12 ... silicon oxide film (etching mask); 13 ... polycrystalline silicon film (thin film); and 14 ... groove.

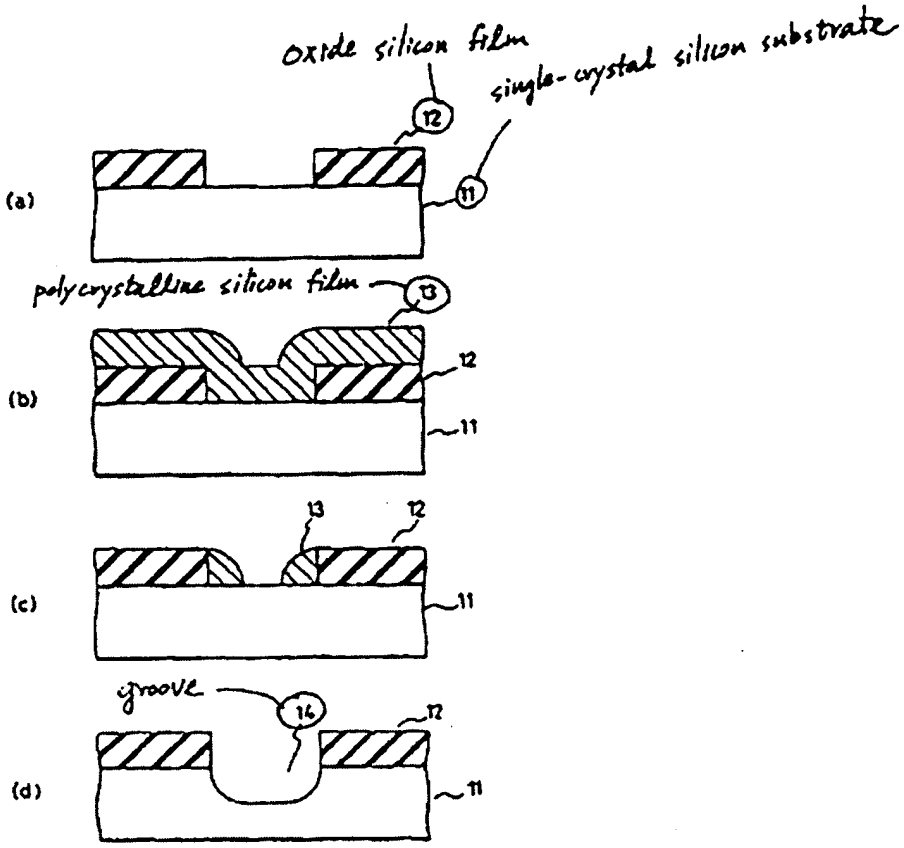

Figure 1

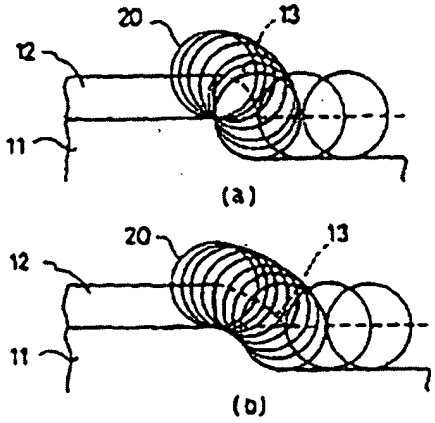

Figure 2

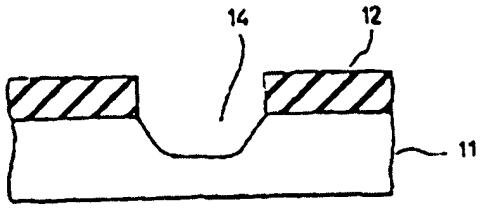

Figure 3

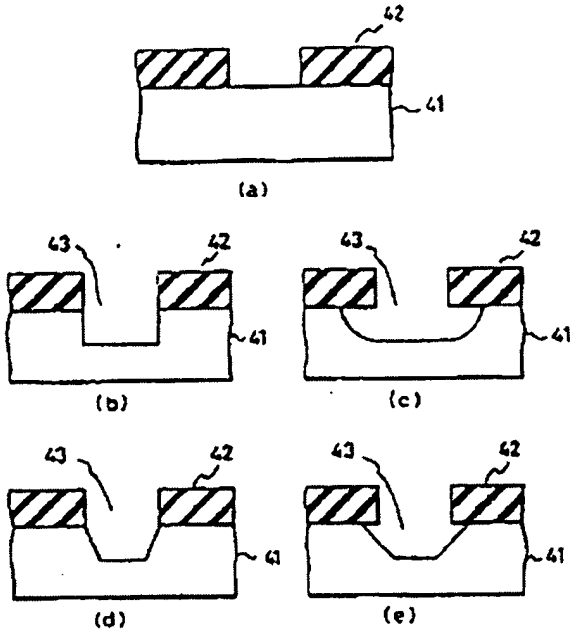

Figure 4